Design and Simulation of Energy Efficient Carbon Nanotube based Digital Circuits

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Abstract: Scaling of silicon technology has led to its curtailed use for high-performance digital circuits. Subsequently, researchers are investigating other novel materials, structures and devices for enhancing circuit performance. Carbon nanotubes (CNTs) have come out as a possibility for the same due to their excellent carrier mobility and faster carrier transport properties. This paper overviews CNTFETs and some compact models. Using the available models, CNT based digital circuits have been analyzed. The parameters like chirality, diameter and threshold voltage for CNTFET and their influence on these parameters on the device characteristics are investigated. A comparative analysis of CMOS and CNTFET logic circuits is carried out. Voltage and current transfer characteristics of CNTFET inverter are presented. Performance metrics viz. delay, power and power delay product (PDP) are analyzed. It is found that CNTFET based circuits are energy efficient. All the circuits have been simulated on HSPICE circuit simulator tool for 32nm technology node.

Key Words: Carbon nanotube (CNT), CNTFET, inverter.

1. INTRODUCTION

Performance enhancement of electronic systems has always attracted the attention of researchers. As a result, Electronics device, technology and circuit researchers are exploring possible alternatives for the future of semiconductor industry. High-mobility transistor channel materials such as III–V compound semiconductors (GaAs, InP etc.) are found to be good alternative. One-dimensional structures e.g., nanowires and carbon nanotubes (CNTs) are also being explored for an active contribution towards electronic system design. CNTs, with their superior carrier mobility, have emerged as a potential candidate to assist the Si technology roadmap in a post 2015 time frame [1]. However, numerous challenges remain. Hence, carbon nanotube field-effect transistors (CNTFETs) provide opportunity for research both the device and circuit levels. CNTFET spans application in various fields’ namely digital inverter, analog designing, amplifiers design etc. [12-14].

This paper briefly presents of carbon nanotube in a nutshell [2-4]. The characteristics of CNTFET inherit characteristics very similar to those of metal oxide semiconductor field effect transistor (MOSFET). Analysis of CNTFET inverter has been detailed. DC voltage transfer and current transfer characteristics of a CNTFET inverter are presented. Variation of power_delay_product (PDP) with load capacitor for CNTFET inverter has been studied. Using more digital logic circuits like NAND, NOR and XOR circuits, a comparative study has been carried out between CMOS technology and CNTFET technologies.

The paper is organized in the following manner. Carbon nanotubes along with their classification and important parameters are presented in section 2. Section 3 demonstrates the design of basic gates using CNTFETs and their performance analysis. Power, delay and power_delay_product decide the performance of the circuits. Conclusions are drawn in section 4.

2. CARBON NANOTUBES

Carbon nanotubes are ultra-fine unique devices, which can offer significant advantages over many existing nanostructured materials due to their remarkable mechanical, electronic and chemical properties. Carbon nanotubes obey quantum mechanics process for carrier transport phenomena.

Carbon nanotubes (CNTs) are sheets of graphene rolled into tubes. Depending on the chirality (i.e., the direction in which the graphene sheet is rolled), a single-walled carbon nanotube (SWCNT) can be either
metallic or semiconducting. This unique property of the SWCNT is referred to as chirality vector and represented by the integer pair \((n,m)\), called the indexes. The nanotube is metallic if \(n=m\) or \(n-m=3i\), where \(i\) is integer. If this condition is not met then the nanotube is semiconducting. When more than one graphene sheets are concentrically rolled then it gives multi-walled carbon nanotubes (MWCNT). Further, CNTs can also be classified on the basis of its structure as zigzag, armchair and chiral nanotube. For chiral integer \(m=0\), is a zigzag structure, with \(n=m\) it gives an armchair structure and for different values of chiral integer \((n,m)\) a chiral nanotube can be obtained. Fig.1 shows these different carbon nanotube atomic structures.

![Figure 1. Atomic structure of carbon nanotubes](image)

The CNT channel region is undoped, while the other regions are heavily doped, thus acting as the source/drain extended region and/or interconnects between two adjacent devices. The conductivity of these undoped regions is controlled by the gate. A ballistic or near-ballistic transport can be obtained under low voltage bias with CNTs due to the ultralong (1µm) mean free path (MFP) of CNTs for elastic scattering [2,3]. By positioning additional CNTs, a linear increase in current can be achieved. However, depending on the distance between CNTs (pitch) and the diameter of each CNT, the current cannot be increased linearly with the number of CNTs in a CNTFET. This is because a small pitch causes the so-called screening effect to occur and the diameter determines the amount of current in a CNT [3, 4].

An undoped carbon nanotube is inserted in channel, whereas the other regions namely source and drain are heavily doped. For a MOSFET like CNTFET, behavior of both positive-FET (pFET) and negative-FET (nFET) are similar. The current density of carbon nanotube (CNT) is very high about 10µA/nm² [10]. Also, CNT has higher carrier velocity with ballistic transport \((v_F=8\times10^7\text{ cm/s})\) [3]. Ballistic transport is a current transport mechanism in which the very same electron that enters one side of the tube appears at the other side.

A MOSFET like CNTFET operates on the principle of barrier height modulation with the application of gate potential. The energy bandgap \((E_G)\) of CNTFET is inversely proportional to the diameter of CNT \((D_{CNT})\) and is given as [3].

\[
E_G = \frac{0.84}{D_{CNT}}
\]

\[
D_{CNT} = \frac{a\sqrt{m^2 + mn + n^2}}{\pi}
\]

where, \(a=0.249\text{nm}\) is lattice constant, \(m\) and \(n\) are integers giving the chiral vector of CNT.

There are three current sources in CNTFET model; viz (i) thermionic current contribution by semiconducting subbands, (ii) the current contribution by metallic subband, and (iii) leakage current caused by band-to-band tunneling mechanism [3].
For conduction to start, the barrier at source channel junction has to be overcome energy $E_G/2 (=\Delta_1$), say). As barrier height determines the threshold voltage of an FET, the threshold voltage ($V_{th}$) in volts of CNTFET is given as [3]

$$V_{th} = \frac{0.42}{D_{CNT}}$$  \hspace{1cm} (3)

The drain current ($I_D$) in CNT is given as [2, 3]

$$I_D = \frac{4eK_BT}{h} \left[ \ln(1 + \exp(-\xi_S)) - \ln(1 + \exp(-\xi_D)) \right]$$  \hspace{1cm} (4)

where $K_B$, $T$ and $h$ are Boltzmann constant, equilibrium temperature and Planck’s constant respectively.

$$\xi_i = \left( \psi - \Delta_1 - \mu_i \right) / K_BT$$  \hspace{1cm} (5)

$\xi_i$ is a constant for $i = S, D$, $\Delta_1$ is half the band gap of CNTFET, $\psi$ is the surface potential and $\mu_i$ is Fermi level.

### 3. RESULTS AND DISCUSSION

In this section, the results obtained and their implications are presented. SPICE compatible carbon nanotube model [7] is used for circuit simulations in HSPICE [8]. CMOS as well as CNTFET inverter, NAND, NOR and XOR circuits are considered and are compared with respective CNTFET circuits. The circuits have been simulated using 32nm technology for minimum dimensions namely channel length $L = (2\lambda) = 32nm$ and $W_n = (3\lambda) = 48nm$ for nMOS. For symmetrical circuit design $W_p = (3W_n) = 144nm$ for pMOS. The nFET and pFET in an inverter are sized as $w_p = 3w_n$ to give the same rising delay and falling delay so that only one transition edge needs to be considered. However, the length and width dimensions for nCNTFET and pCNTFET are identical.

#### 3.1 Analyses of CNTFET inverter

Complementary metal oxide semiconductor (CMOS) inverter has gained an immense importance with time. CMOS inverter has two important advantages over the other inverter configurations like resistive load inverter, pseudo nMOS inverter etc. The first advantage is that the CMOS inverter circuit dissipates negligible steady-state power, except for the small power dissipation due to leakage currents. The other advantage is that CMOS exhibits full output voltage swing from 0V to supply voltage ($V_{DD}$). Voltage transfer characteristic (VTC) transition is usually quite sharp which resembles that of an ideal inverter. Since nMOS and pMOS transistors must be fabricated on the same chip side-by-side, the CMOS fabrication process is more complex than the standard nMOS-only process. In particular, the CMOS process must provide an n-type substrate for the pMOS transistors and a p-type substrate for the nMOS transistors [9].

With down scaling of channel length of a MOS transistor non-ideal effects like drain induced barrier lowering (DIBL), gate induced drain leakage (GIDL), mobility degradation, velocity saturation etc. have become adverse. Hence, circuit designers have explored carbon nanotube field effect transistor (CNTFET) as a solution to overcome these drawbacks. As it replicated the characteristics of a MOSFET, complementary CNTFET inverter is also designed. The circuits are simulated using CNTFET using HSPICE. The device parameters and process assumptions taken for CNTFET are given in Table I [4].

<table>
<thead>
<tr>
<th>Variable Parameters</th>
<th>Source/Drain Doping Level</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>0.59 eV - 0.75 eV (0.7%- 1.3%)</td>
</tr>
</tbody>
</table>
### CNT Diameter
1.2 nm - 1.8 nm

### Probability of a CNT to be Metallic
8% - 32%

### Fixed Parameters

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
</thead>
<tbody>
<tr>
<td>Oxide Thickness ($T_{ox}$)</td>
<td>4 nm</td>
</tr>
<tr>
<td>Gate Dielectric (Dielectric Constant:$K_{ox}$)</td>
<td>HfO$_2$ (16)</td>
</tr>
<tr>
<td>CNT Pitch</td>
<td>4 nm</td>
</tr>
<tr>
<td>Gate Length (CNT)</td>
<td>32 nm</td>
</tr>
<tr>
<td>Work Function: contact ($\Phi_M$)</td>
<td>4.5 eV</td>
</tr>
<tr>
<td>Work Function: CNT ($\Phi_{CNT}$)</td>
<td>4.5 eV</td>
</tr>
</tbody>
</table>

Figure 2. Shows the schematic of a typical CNTFET inverter. The DC voltage transfer characteristics for CMOS and CNTFET inverters are shown in Fig. 3. It can be observed that both attain the voltage transfer characteristic (VTC) of an inverter. CNTFET inverter leads to steeper VTC, which is nearer to the desired ideal VTC with a sharp transition. Thus, the VTC of the CNTFET inverter resembles that of an ideal inverter more closely [9].

Figure 3. Schematic of a CNTFET inverter circuit.

Figure 4. DC voltage transfer characteristics (VTC) of (a) CMOS inverter and (b) CNTFET inverter.
Na et al. [6] has shown that the choice of effective drain current \( I_{\text{eff}} = \frac{I_H + I_L}{2} \), where \( I_L = I_{DS}(V_{GS} = V_{DD}/2, V_{DS} = V_{DD}) \) and \( I_H = I_{DS}(V_{GS} = V_{DD}, V_{DS} = V_{DD}/2) \), has better correlation with inverter gate delay than \( I_{DS} \). The ratio of the “turning off” current, which flows through the device that is being turned off, to the “turning on” current \( \frac{I_{\text{off}}}{I_{\text{on}}} \) is constant from 50% to 50%. This implies that the “turning off” current is relatively small compared to the “turning on” current. The “turning on” current trajectory of CNTFET which is bounded by the \( I_{DS} \) versus \( V_{DS} \) curve does not resemble with silicon devices. The “turning off” current for short channel device becomes more significant [3, 4]. The current transfer characteristics curve is obtained from Avanwaves tool of HSPICE circuit simulator [8] and is shown in Fig. 4.

Power_delay_product (PDP) represents the energy dissipated by a circuit and should have minimum value. PDP for varying load capacitance of CNTFET inverter is given in Fig. 5. It is seen from figure that PDP increases with load capacitance. It is least for loads less than 20fF.

### 3.2 Parametric analysis of CNTFET based digital circuits

CNTFET inverter, NAND, NOR and XOR circuits are simulated using CNTFET model file [7] and HSPICE [8] for 32nm technology. The performance parameters viz. power, delay and power_delay_product (PDP) have been determined for these circuits as well as for the CMOS circuit designs.

Table II illustrates that both power and delay are reduced in case of CNTFET circuits. PDP for CNTFET circuits is lower than CMOS circuits. For instance PDP is 0.72aJ, 7.19aJ, 7.774aJ and 13.85aJ for CNTFET inverter, NAND, NOR and XOR circuits respectively. Lower PDP represents lower energy dissipation. Hence, it is inferred that CNTFET circuits are more energy efficient than CMOS counterparts.
A CNTFET inverter circuit provides 84.84% power reduction, 76.52% delay reduction and 96.44% PDP reduction when compared to CMOS inverter circuit. As compared to CMOS NAND and XOR circuit 40.22% and 54.74% delay reduction is noticed for CNTFET circuits. In a similar manner a reduction in power of 86%, 78.26% and 82.54% and reduction in PDP of 91.61%, 75.36% and 92.10% is achieved for CNTFET based NAND, NOR and XOR digital circuits respectively.

4. CONCLUSION

A comparative analysis of CMOS and CNTFET inverters is presented. Voltage and current transfer characteristics of CNTFET inverter are presented. It is observed that CNTFET based digital circuits namely inverter, NAND, NOR and XOR exhibits lesser power dissipation, propagation delay as well as PDP. On an average the CNTFET circuits provide 57.16% lesser delay, 82.91% lower power dissipation and 88.88% lesser PDP than the corresponding CMOS circuits.

Hence, it can be summarized that CNTFET based digital logic circuits are energy efficient and thus a low power solution for digital circuit design applications.

REFERENCES


